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EXAMINER	
PERKINS, PAMELA E	

ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,097	DORIS ET AL.	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *12-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date [redacted]
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the applications papers on 26 June 2003. Claims 1-18 are pending.

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-11, drawn to a method of manufacturing a semiconductor device, classified in class 438, subclass 270.

II. Claims 12-18, drawn to a semiconductor device, classified in class 257, subclass 330.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed can be made by another and materially different process. For example, the product does not require the FET device to have a height less than the height of the FinFET as required in the process.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Leslie Szivos on 13 July 2004 a provisional election was made without traverse to prosecute the invention of group I, claims 1-11. Affirmation of this election must be made by applicant in replying to this Office action. Claims 12-18 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 5, 7, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. (6,252,284) in view of Ono (6,166,413).

Mullet al. disclose a method of forming an integrated semiconductor circuit where a silicon-on-insulator structure (5) comprises at least a top semiconductor layer located on a buried insulating layer (col. 6, lines 17-33), the top semiconductor layer having at least one patterned hard mask (40) located in a FinFET region of the structure (5) and

at least one patterned hard mask (44) located in a FET region of the structure (col. 5, lines 45-58); protecting the FET region and trimming the at least one patterned hard mask in the FinFET region, wherein the protecting the FET region comprising applying a resist mask (44) to the FET region (col. 6, lines 18-32); etching exposed portions of the top semiconductor that are not protected with the hard masks stopping on the buried insulating layer, the etching defining a FinFET active device region and a FET active device region, the FinFET active device region being perpendicular to the FET active device region (Fig. 1 & 14; col. 6, lines 18-59); forming a gate dielectric (12) on each exposed vertical surface of the FinFET active device region, while forming a gate dielectric (20) on an exposed horizontal surface of the FET device region (Fig. 7A & 7B; col. 6, lines 60-67); forming a patterned gate electrode (21) on each exposed surface of the gate dielectric (12/20) (col. 6, line 67 thru col. 7, line 20); and forming spacers (23) abutting the patterned gate electrode (21) (Fig. 10B; col. 7,lines 21-34)

Muller et al. further disclose the trimming including a chemical oxide removal process or a wet etch process. Muller et al. also disclose forming the patterned gate electrodes by depositing a gate conductor material; forming a patterned resist on top of the gate conductor material; and etching exposed portions of the gate conductor not protected with the patterned resist. Muller et al. do not disclose protecting the FinFET active device region and thinning the FET active device region so that the FET device region has a height that is less than the height of the FinFET active device region, wherein the protecting the FinFET active device region comprises applying a resist mask to the FinFET active device region

Ono discloses a method of forming an integrated semiconductor circuit where a silicon structure (20) comprises at least a top semiconductor layer, the top semiconductor layer having at least one patterned hard mask (25c) located in a first FET region (22) of the structure (20) and at least one patterned hard mask (25b) located in a second FET region (23) of the structure (20) (Fig. 2E & 2H; col. 7, line 41 thru col. 8, line 15); protecting the second FET region (22) and trimming the at least one patterned hard mask in the first FET region (23), wherein the protecting the second FET region (22) comprising applying a resist mask (25c) to the second FET region (22) (Fig. 2H & 2I; col. 7, lines 6-23); protecting the first FET active device region (23) and thinning the second FET active device region (22) so that the second FET device region (22) has a height that is less than the height of the first FET active device region (23), wherein the protecting the first FET active device region (23) comprises applying a resist mask (25b) to the first FET active device region (23) (Fig. 2E-2G; col. 7, line 41 thru col. 8, line 15); etching exposed portions of the top semiconductor that are not protected with the hard masks, the etching defining a first FET active device region (23) and a second FET active device region (22) (FIG. 2C; col. 7, line 8-23); forming a gate dielectric (22a/23a) on an exposed horizontal surface of the first and second FET device regions (23/22) (Fig. 2B; col. 6, lines 25-57); forming a patterned gate electrode (22b/23b) on each exposed surface of the gate dielectric (22a/23a) (FIG. 2C; col. 7, lines 23-50); and forming spacers (22c/23c) abutting the patterned gate electrode (22b/23b) (Fig. 2D; col. 7, lines 8-34).

Ono further discloses the thinning including an etching process that is highly selective to SiO_2 (col. 7, lines 41-65). Ono also discloses the patterned hard masks are formed by the steps of: forming an oxide layer on a surface of the top semiconductor layer; forming a mask layer on the oxide layer; applying a photoresist to an exposed surface of the mask layer; exposing the photoresist to a pattern of radiation; developing the pattern into the photoresist; and transferring the pattern from the photoresist into the mask layer and the oxide layer (col. 6, line 66 thru col. 7, line 8).

Since Muller et al. and Ono are both from the same field of endeavor, a method of forming an integrated semiconductor circuit, the purpose disclosed by Ono would have been recognized in the pertinent art of Muller et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Ono by protecting the FinFET active device region and thinning the FET active device region so that the FET device region has a height that is less than the height of the FinFET active device region, wherein the protecting the FinFET active device region comprises applying a resist mask to the FinFET active device region as taught by Ono to prevent diffusion into the channel region (col. 4, line 37 thru col. 5, line 3).

Claims 6, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller et al. in view of Ono as applied to claim 1 above, and further in view of Fried et al. (6,657,259).

Muller et al. in view of Ono disclose the subject matter claimed above except the FinFET active device region having a (100) or (110) surface orientation, the FET active

device region having a (100) or (11) surface orientation and forming the gate dielectric as an oxide by a thermal oxidation process.

Fried et al. disclose a method of forming an integrated semiconductor circuit where a silicon-on-insulator structure (200) comprises at least a top semiconductor layer (206) located on a buried insulating layer (204) (col. 7, lines 17-67), the top semiconductor layer (206) having at least one patterned hard mask (208) located in a FinFET region of the structure (200) (col. 8, lines 1-40); trimming the at least one patterned hard mask (208) in the FinFET region (col. 8, lines 31-40); etching exposed portions of the top semiconductor (206) that are not protected with the hard masks (208) stopping on the buried insulating layer (204), the etching defining a FinFET active device region (Fig. 4b; col. 8, lines 41-49), FinFET active device region being perpendicular to a FET active device region (Fig. 7a; col. 10, lines 18-65); forming a gate dielectric (210) on each exposed vertical surface of the FinFET active device region (Fig. 5b; col. 9, lines 52-62); and forming a patterned gate electrode (212) on each exposed surface of the gate dielectric (210) (Fig. 7b; col. 10, lines 18-65). Yu further discloses the FinFET active device region having a (100) or (110) surface orientation, the FET active device region having a (100) or (11) surface orientation (col. 5, lines 50-64; col. 6, lines 52-64) and forming the gate dielectric (210) as an oxide by a thermal oxidation process (col. 9, lines 52-62).

Since Muller et al. and Fried et al. are both from the same field of endeavor, a method of forming an integrated semiconductor circuit, the purpose disclosed by Fried et al. would have been recognized in the pertinent art of Muller et al. Therefore, it would

have been obvious to one ordinary skill in the art at the time the invention was made to modify Muller et al. by the FinFET active device region having a (100) or (110) surface orientation, the FET active device region having a (100) or (11) surface orientation and forming the gate dielectric as an oxide by a thermal oxidation process as taught by Fired et al. to optimize carrier mobility's (col. 2, lines 48-62).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Abadeer et al. (JP 2004-088101), Yu (6,300,182) and Hu et al. (6,413,802) all disclose a method of forming an integrated semiconductor circuit where a silicon-on-insulator structure comprises at least a top semiconductor layer located on a buried insulating layer, the top semiconductor layer having at least one patterned hard mask located in a FinFET region of the structure and at least one patterned hard mask located in a FET region of the structure; protecting the FET region and trimming the at least one patterned hard mask in the FinFET region, wherein the protecting the FET region comprising applying a resist mask to the FET region; etching exposed portions of the top semiconductor that are not protected with the hard masks stopping on the buried insulating layer, the etching defining a FinFET active device region and a FET active device region, the FinFET active device region being perpendicular to the FET active device region; forming a gate dielectric on each exposed vertical surface of the FinFET active device region, while forming a gate dielectric on an exposed horizontal surface of

the FET device region; forming a patterned gate electrode on each exposed surface of the gate dielectric; and forming spacers abutting the patterned gate electrode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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